Route design DRC

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| Tool Version : Vivado v.2021.1 (win64) Build 3247384 Thu Jun 10 19:36:33 MDT 2021

| Date : Wed Apr 10 16:12:11 2024

| Host : DESKTOP-4LK3EFH running 64-bit major release (build 9200)

| Command : report\_drc -file UART\_drc\_routed.rpt -pb UART\_drc\_routed.pb -rpx UART\_drc\_routed.rpx

| Design : UART

| Device : xc7z020clg400-1

| Speed File : -1

| Design State : Fully Routed

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Report DRC

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1. REPORT SUMMARY

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Netlist: netlist

Floorplan: design\_1

Design limits: <entire design considered>

Ruledeck: default

Max violations: <unlimited>

Violations found: 1

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| Rule | Severity | Description | Violations |

+--------+----------+--------------------+------------+

| ZPS7-1 | Warning | PS7 block required | 1 |

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2. REPORT DETAILS

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ZPS7-1#1 Warning

PS7 block required

The PS7 cell must be used in this Zynq design in order to enable correct default configuration.

Related violations: <none>